CHARACTERIZATION OF W-BAND MMIC POWER AMPLIFIER USING ON-WAFER PULSED POWER TEST*

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ABSTRACT

A facile technique based on pulsed power test has been developed to characterize W-Band MMIC power amplifiers and optimize their gain and PAE (power added efficiency) *on-wafer* By suppressing thermal effects usually associated with conventional on-wafer tests, the pulsed power technique makes it possible to not only establish device binning criteria but also eliminate in-module bias tuning. It thus provides significant cost savings in volume production environments.

INTRODUCTION

On-wafer test are regularly used to verify MMIC circuit functionalities. However, normal CW on-wafer technique often cannot accurately measure important parameters, such as maximum output power (P_{out}), PAE, and current under drive, due to thermal considerations. This shortcoming is particular acute in millimeter wave power amplifiers, where a lack of suitable testing technique makes it necessary to have the device first mounted in the module assembly, and then bias tuned for optimum performance, at significant time and cost penalties.

Pulsed on-wafer measurement with gate bias optimization readily eliminates inadvertent thermal effects and has been successfully applied to Ka-band power amplifiers [1, 2] At W-band frequencies, this technique becomes even more valuable for MMIC power amplifiers in light of higher chip process variations and reduced device size.

We report here the successful extension of pulsed on-wafer test methodology to W-band devices, and the procedure whereby key parameters, including device gain, output power, PAE, optimum gate bias, and drain current under drive can be obtained.

TEST SETUP

The scalar test setup used in this study is shown in Fig. 1. A synthesized source with multiplier is used to generate the W-band test signal. The power level is controlled by a programmable attenuator, which is in turn connected to a power amplifier module capable of providing 30 dB gain and +26 dBm of output power to allow maximum test signal power be delivered to the DUT (device under test). The test signal levels at input and output ports are monitored with separate power meters. Since pulsed power meters are not

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commercially available at this frequency, a calibration table was first generated to correlate the power meter reading with the actual peak power during the testset calibration. Each of the passive components in the setup is characterized with a vector network analyzer to correct for insertion loss. A custom-made pulser is used to supply the bias to the drain while the gate bias is kept constant. An oscilloscope is used to monitor the drain voltage and current while the RF test signal is applied.

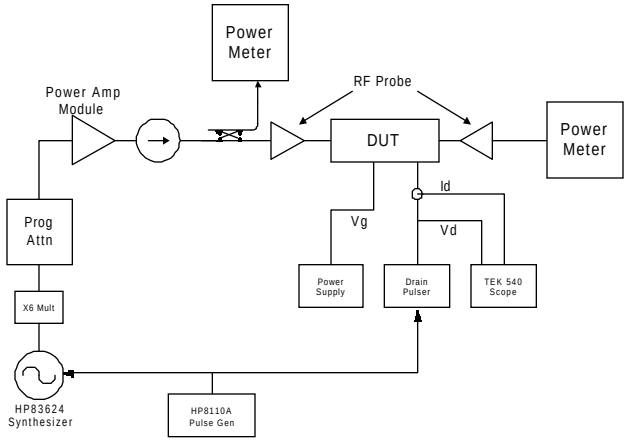

Fig. 1 W-band On-Wafer Pulsed Power Scalar Test Setup Block Diagram

To optimize circuit performance, the test software ramps the gate voltage and records P_{out} vs. V_{gs} at the center frequency with the test signal set at a predetermined level at the input port. Measurement of the drain current under RF drive gave the PAE. Test data are used to derive the optimum gate bias, which in turn is used to measure the P_{in}/P_{out} and PAE over frequency.

TEST METHODOLOGY

A W-band MMIC power amplifier was used to verify this test technique. This test device involves a two stage design on a 2-mil substrate, and is shown in Fig. 2. It has a typical linear gain of 10 dB and a total device periphery of 1.92 mm [3]. To determine the pulse width and duty cycle applicable to on-wafer measurements, several experiments were performed to assess the thermal effects on the device performance, and the results are plotted in Fig. 3. We chose to use 5 microsecond pulses with 2.5% duty cycle for the on-wafer tests. This condition minimized thermal effects, while maintaining good measurement repeatability, especially the power meter readout, under pulsed operation.

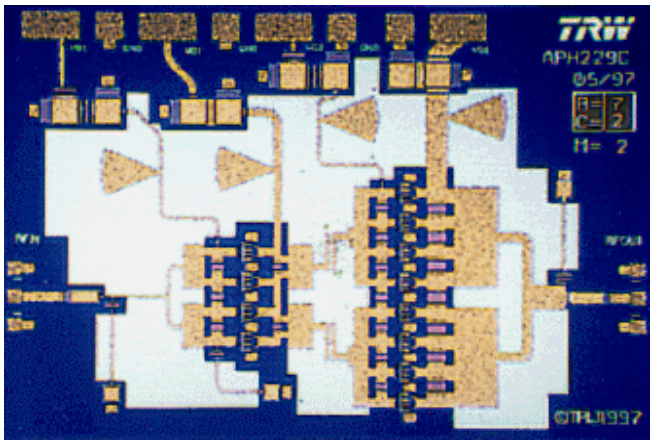

Fig.2 W-band MMIC Power Amplifier Test Circuit

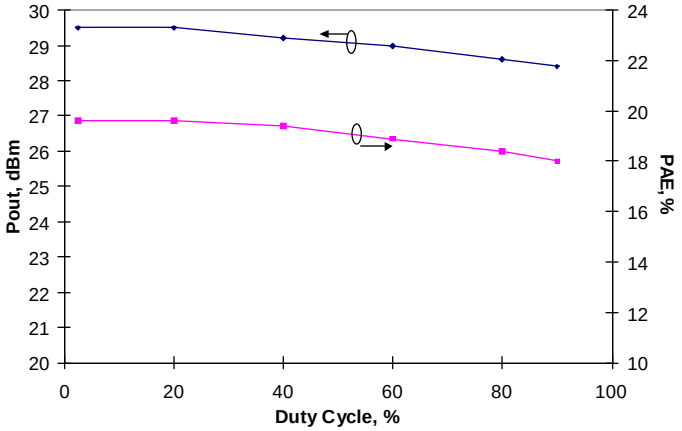

Fig. 3. P_{out} and PAE vs. Duty Cycle

The validity of the pulsed measurement has been established by testing sample circuits in fixture, and the results match on-wafer data

well. More importantly, the pulse technique provides an additional advantage over conventional CW procedure: as shown in Figs. 4 and 5, respectively, both the drain current under RF drive and the P_{out}/PAE are functions of gate bias. Depending on the application, gate bias can be rapidly adjusted (<10 seconds per site - limited by the power meter's response time) on wafer to maximize the circuit performance based on P_{out} and PAE, and the operating bias can also be individually optimized for each chip.

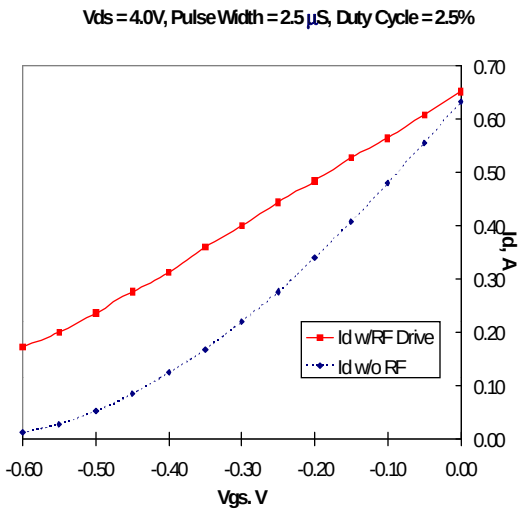

Fig. 4. Drain Current vs. Gate Bias Voltage

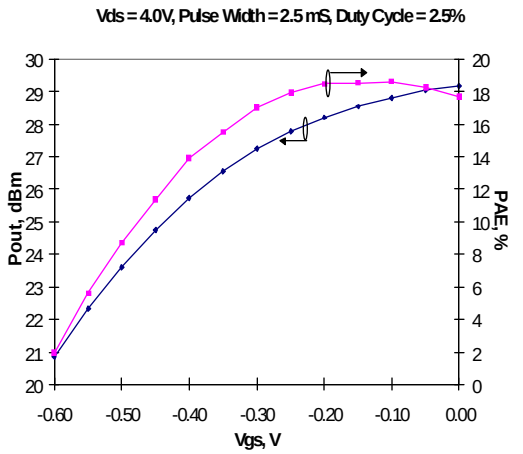

Fig. 5. P_{out} and PAE vs. Gate Bias Voltage

Several lots of wafer have been tested using this technique. Representative P_{in}/P_{out} measurements, made under optimal gate bias and at three frequencies, are shown in Fig. 6, and P_{out} value distribution from a typical wafer is given in Figure 7. Such results are not routinely collected in the past, because test time would be prohibitive.

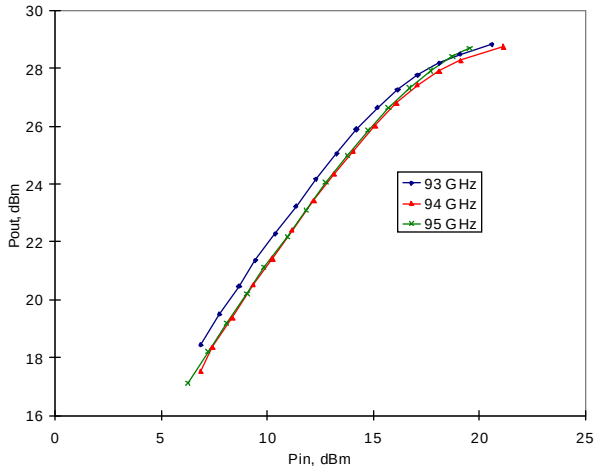

Fig. 6. W-Band Power Amplifier P_{in}/P_{out} Over Frequency

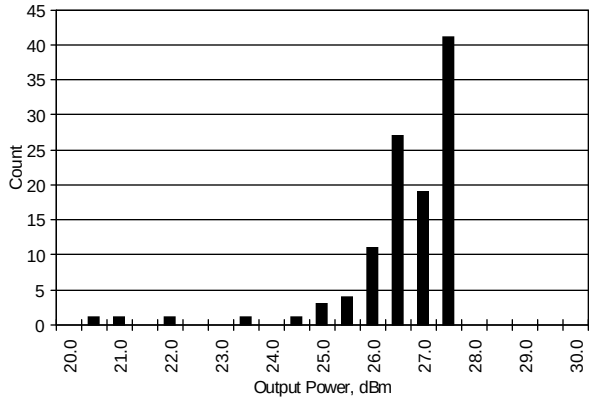

Fig. 7. Typical P_{out} Distribution of a 94 GHz Power Amplifier Wafer

SUMMARY

A pulsed power on-wafer test technique with bias optimization has been successfully developed for W-band application. This approach can be used to determine the MMIC power amplifier P_{out}, PAE, optimum gate bias, and drain current under drive, on-wafer, with

readily available test equipment. It provides a powerful tool to rapidly determine MMIC power amplifier performance.

ACKNOWLEDGMENT

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